

# CS4124

## High Side PWM FET Controller

The CS4124 is a monolithic integrated circuit designed primarily to control the rotor speed of permanent magnet, direct current (DC) brush motors. It drives the gate of an N channel power MOSFET or IGBT with a user-adjustable, fixed frequency, variable duty cycle, pulse width modulated (PWM) signal. The CS4124 can also be used to control other loads such as incandescent bulbs and solenoids. Inductive current from the motor or solenoid is recirculated through an external diode.

The CS4124 accepts a DC level input signal of 0 to 5.0 V to control the pulse width of the output signal. This signal can be generated by a potentiometer referenced to the on-chip 5.0 V linear regulator, or a filtered 0% to 100% PWM signal also referenced to the 5.0 V regulator.

The IC is placed in a sleep state by pulling the CTL lead below 0.5 V. In this mode everything on the chip is shutdown except for the on-chip regulator and the overall current draw is less than 275  $\mu$ A. There are a number of on-chip diagnostics that look for potential failure modes and can disable the external power MOSFET.

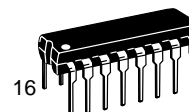
### Features

- 150 mA Peak PWM Gate Drive Output
- Patented Voltage Compensation Circuit
- 100% Duty Cycle Capability
- 5.0 V,  $\pm$  3.0% Linear Regulator
- Low Current Sleep Mode
- Overvoltage Protection
- Boost Mode Power Supply
- Output Inhibit



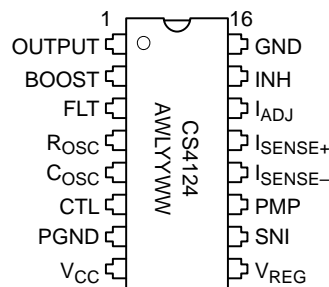
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1  
DIP-16  
N SUFFIX  
CASE 648

### PIN CONNECTION AND MARKING DIAGRAM



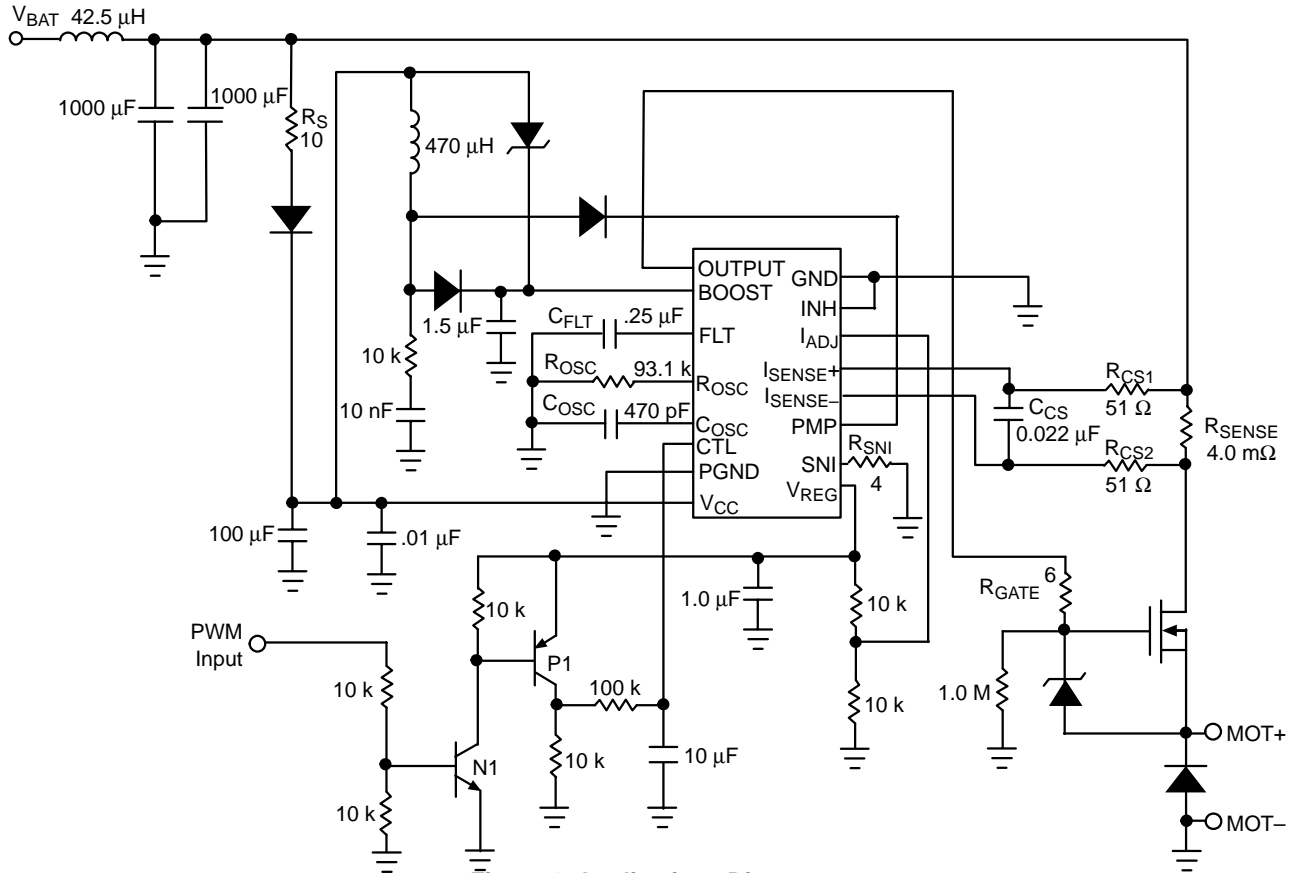
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION\*

Device	Package	Shipping
CS4124YN16	DIP-16	25 Units/Rail

\* Contact your local sales representative for 16-lead SOIC wide package.

# CS4124



**Figure 1. Applications Diagram**

## ABSOLUTE MAXIMUM RATINGS\*

Rating	Value	Unit
Storage Temperature Range	-65 to 150	°C
V <sub>CC</sub>	-0.3 to 30	V
V <sub>CC</sub> Peak Transient Voltage (load dump = 26 V w/ series 10 Ω resistor)	40	V
Input Voltage Range (at any input)	-0.3 to 10	V
Maximum Junction Temperature	150	°C
Lead Temperature Soldering	Wave Solder (through hole styles only) Note 1.	260 peak
ESD Susceptibility (Human Body Model)	2.0	kV

1. 10 seconds max.

\*The maximum package power dissipation must be observed.

# CS4124

## ELECTRICAL CHARACTERISTICS (4.0 V ≤ V<sub>CC</sub> ≤ 26 V; -40°C < T<sub>J</sub> < 125°C; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
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### V<sub>CC</sub> Supply

Operating Current Supply	7.0 V ≤ V <sub>CC</sub> ≤ 18 V	–	5.0	10	mA
	4.0 V ≤ V <sub>CC</sub> < 7.0 V, 18 V < V <sub>CC</sub> ≤ 26 V	–	–	15	mA
Quiescent Current	V <sub>CC</sub> = 12 V	–	170	275	μA
Overshoot Shutdown	–	26.5	–	29	V

### Control (CTL)

Control Input Current	CTL = 0 V to 5.0 V	–2.0	0.1	2.0	μA
Sleep Mode Threshold	–	8.0%	10%	12%	V <sub>REG</sub>
Sleep Mode Hysteresis	7.0 V ≤ V <sub>CC</sub> ≤ 26 V	50	100	150	mV
	4.0 V ≤ V <sub>CC</sub> < 7.0 V	10	–	150	mV

### Control Sense

Differential Voltage Sense	7.0 V ≤ V <sub>CC</sub> ≤ 18 V:				
	I <sub>ADJ</sub> = 1.0 V and R <sub>CS1</sub> = 51 Ω	18	–	34	mV
	I <sub>ADJ</sub> = 4.0 V and R <sub>CS1</sub> = 51 Ω	104	–	125	mV
	4.0 V ≤ V <sub>CC</sub> < 7.0 V:				
	I <sub>ADJ</sub> = 1.0 V and R <sub>CS1</sub> = 51 Ω	15	–	39	mV
	18 V < V <sub>CC</sub> ≤ 26 V:				
I <sub>ADJ</sub> = 1.0 V and R <sub>CS1</sub> = 51 Ω	15	–	39	mV	
I <sub>ADJ</sub> = 4.0 V and R <sub>CS1</sub> = 51 Ω	102	–	130	mV	
I <sub>ADJ</sub> Input Current	4.0 V ≤ V <sub>CC</sub> ≤ 26 V, I <sub>ADJ</sub> = 0 V to 5.0 V	–2.0	0.3	2.0	μA

### Linear Regulator

Output Voltage, V <sub>REG</sub>	V <sub>CC</sub> = 4.0 V	2.0	–	–	V
	V <sub>CC</sub> = 13.2 V	4.85	–	5.15	V
	V <sub>CC</sub> = 26 V	4.85	–	5.20	V

### Inhibit

Inhibit Threshold	–	40%	50%	60%	V <sub>REG</sub>
Inhibit Hysteresis	4.0 V ≤ V <sub>CC</sub> ≤ 7.0 V	100	–	500	mV
	7.0 V ≤ V <sub>CC</sub> ≤ 26 V	150	325	500	mV

### External Drive (OUTPUT)

Output Frequency	4.0 V ≤ V <sub>CC</sub> < 7.0 V:				
	R <sub>OSC</sub> = 93.1 kΩ, C <sub>OSC</sub> = 470 pF	10	–	25	kHz
	7.0 V ≤ V <sub>CC</sub> ≤ 18 V:				
R <sub>OSC</sub> = 93.1 kΩ, C <sub>OSC</sub> = 470 pF	17	20	23	kHz	
18 V < V <sub>CC</sub> ≤ 26 V:					
R <sub>OSC</sub> = 93.1 kΩ, C <sub>OSC</sub> = 470 pF	17	20	25	kHz	
Voltage to Duty Cycle Conversion	4.0 V ≤ V <sub>CC</sub> < 7.0 V:				
	V <sub>CC</sub> = 13 V, CTL = 1.0 V	65	–	75	%
	V <sub>CC</sub> = 13 V, CTL = 2.0 V	100	–	–	%
	7.0 V ≤ V <sub>CC</sub> ≤ 18 V:				
	V <sub>CC</sub> = 13 V, CTL = 30% V <sub>REG</sub>	28.3	–	36.3	%
	V <sub>CC</sub> = 13 V, CTL = 55.8% V <sub>REG</sub>	56.0	–	64.0	%
	18 V < V <sub>CC</sub> ≤ 26 V:				
	V <sub>CC</sub> = 13 V, CTL = 1.5 V	11.8	–	21.8	%
V <sub>CC</sub> = 13 V, CTL = 3.5 V	34.2	–	44.2	%	
Output Rise Time	4.0 V ≤ V <sub>CC</sub> ≤ 26 V: R <sub>GATE</sub> = 6.0 Ω, C <sub>GATE</sub> = 5.0 nF	–	.25	1.0	μs
Output Fall Time	4.0 V ≤ V <sub>CC</sub> ≤ 26 V: R <sub>GATE</sub> = 6.0 Ω, C <sub>GATE</sub> = 5.0 nF	–	.30	1.0	μs

# CS4124

## ELECTRICAL CHARACTERISTICS (continued) (4.0 V ≤ V<sub>CC</sub> ≤ 26 V; -40°C < T<sub>J</sub> < 125°C; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
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### External Drive (OUTPUT) (continued)

Output Sink Current	4.0 V ≤ V <sub>CC</sub> < 7.0 V: R <sub>GATE</sub> = 6.0 Ω, C <sub>GATE</sub> = 5.0 nF	-	150	-	mA
	7.0 V ≤ V <sub>CC</sub> ≤ 26 V: R <sub>GATE</sub> = 6.0 Ω, C <sub>GATE</sub> = 5.0 nF	-	300	-	mA
Output Source Current	4.0 V ≤ V <sub>CC</sub> < 7.0 V: R <sub>GATE</sub> = 6.0 Ω, C <sub>GATE</sub> = 5.0 nF	-	150	-	mA
	7.0 V ≤ V <sub>CC</sub> ≤ 26 V: R <sub>GATE</sub> = 6.0 Ω, C <sub>GATE</sub> = 5.0 nF	-	300	-	mA
Output High Voltage	I <sub>OUT</sub> = 1.0 mA	V <sub>BOOST</sub> = 1.7	-	-	V
Output Low Voltage	I <sub>OUT</sub> = -1.0 mA	-	-	1.3	V

### Charge Pump (DRV)

Boost Voltage	-	V <sub>CC</sub> + 6.4	-	-	V
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## PIN FUNCTION DESCRIPTION

PACKAGE PIN #		
16 Lead PDIP	PIN SYMBOL	FUNCTION
1	OUTPUT	MOSFET gate drive.
2	BOOST	Boost voltage.
3	FLT	Fault time out capacitor.
4	R <sub>OSC</sub>	Oscillator resistor.
5	C <sub>OSC</sub>	Oscillator capacitor.
6	CTL	Pulse width control input.
7	PGND	Power ground for on chip clamp.
8	V <sub>CC</sub>	Positive power supply input.
9	V <sub>REG</sub>	5.0 V linear regulator.
10	SNI	Sense inductor current.
11	PMP	Collector of boost power transistor.
12	I <sub>SENSE-</sub>	Current sense minus.
13	I <sub>SENSE+</sub>	Current sense plus.
14	I <sub>ADJ</sub>	Current limit adjust.
15	INH	Output Inhibit.
16	GND	Ground.

# CS4124

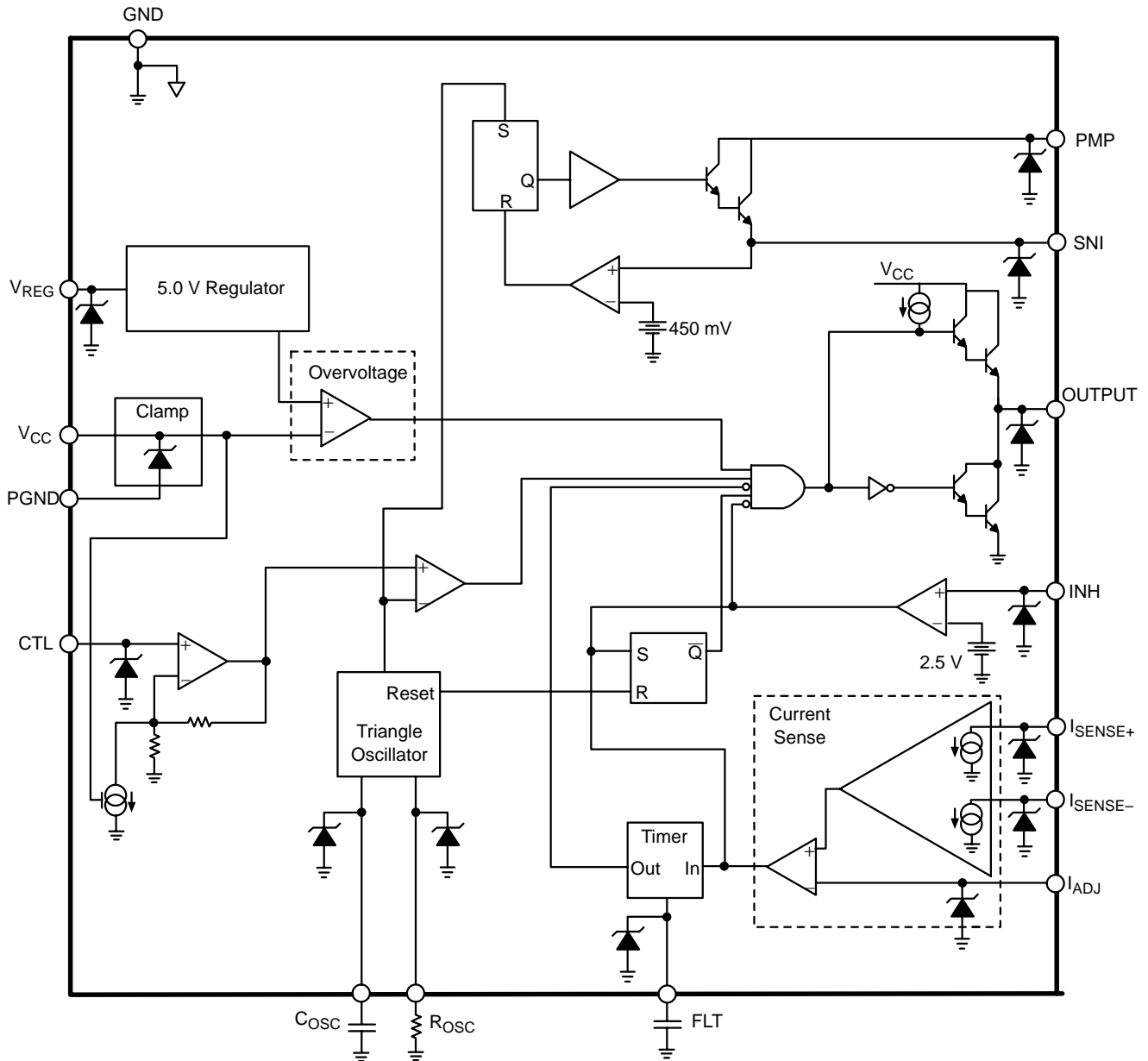


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

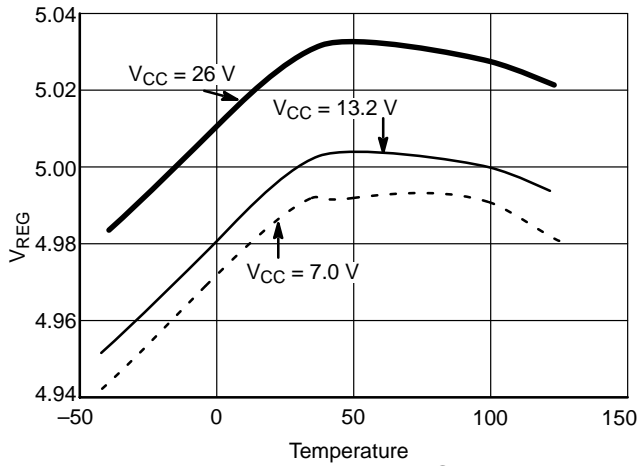


Figure 3.  $V_{REG}$  vs. Temperature @  $I_{LOAD} = 5.0\text{ mA}$

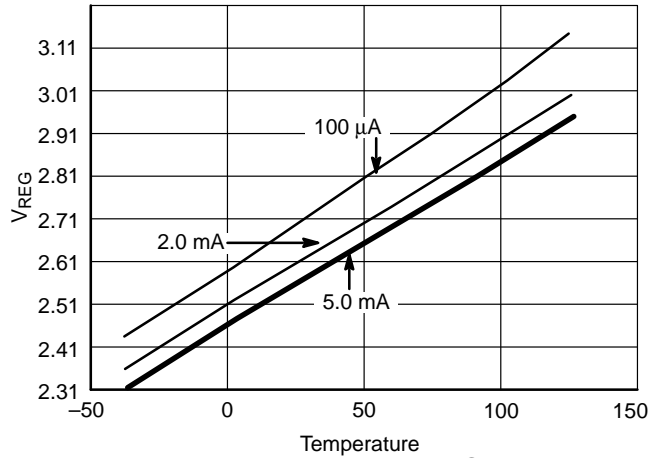


Figure 4.  $V_{REG}$  vs. Temperature @  $V_{CC} = 4.0\text{ V}$

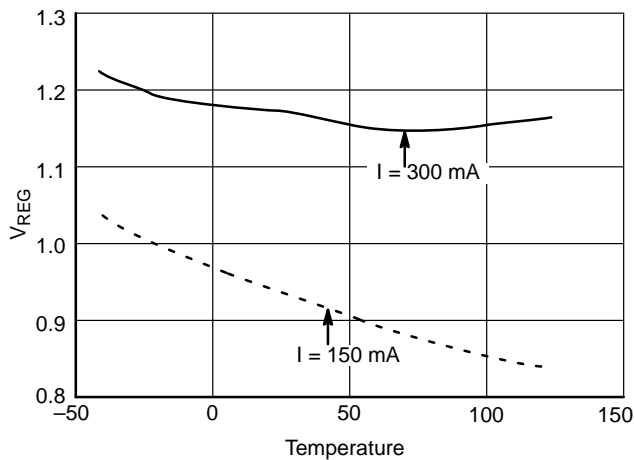


Figure 5. OUTPUT Voltage (Sinking Current) vs. Temperature

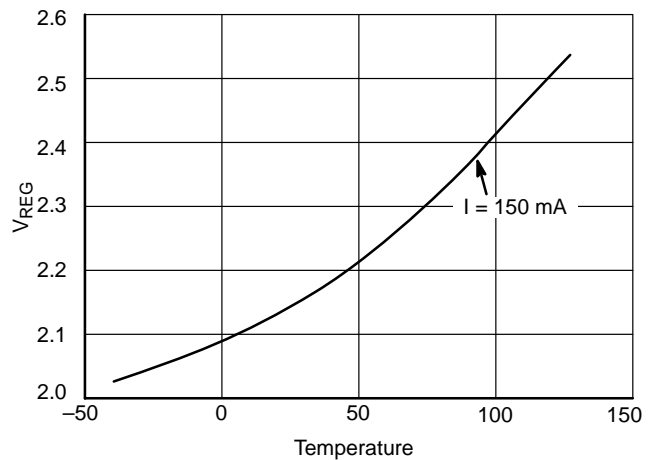


Figure 6. OUTPUT Saturation Voltage (Sourcing Current) vs. Temperature

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## Oscillator

The IC sets up a constant frequency triangle wave at the  $C_{OSC}$  lead whose frequency is related to the external components  $R_{OSC}$  and  $C_{OSC}$ , by the following equation:

$$\text{Frequency} = \frac{0.83}{R_{OSC} \times C_{OSC}}$$

The peak and valley of the triangle wave are proportional to  $V_{CC}$  by the following:

$$V_{VALLEY} = 0.1 \times V_{CC}$$

$$V_{PEAK} = 0.7 \times V_{CC}$$

This is required to make the voltage compensation function properly. In order to keep the frequency of the oscillator constant the current that charges  $C_{OSC}$  must also vary with supply.  $R_{OSC}$  sets up the current which charges  $C_{OSC}$ . The voltage across  $R_{OSC}$  is 50% of  $V_{CC}$  and therefore:

$$I_{ROSC} = 0.5 \times \frac{V_{CC}}{R_{OSC}}$$

$I_{ROSC}$  is multiplied by (2) internally and transferred to the  $C_{OSC}$  lead. Therefore:

$$I_{COSC} = \pm \frac{V_{CC}}{R_{OSC}}$$

The period of the oscillator is:

$$T = 2C_{OSC} \times \frac{V_{PEAK} - V_{VALLEY}}{I_{COSC}}$$

The  $R_{OSC}$  and  $C_{OSC}$  components can be varied to create frequencies over the range of 15 Hz to 25 kHz. With the suggested values of 93.1 k $\Omega$  and 470 pF for  $R_{OSC}$  and  $C_{OSC}$ , the nominal frequency will be approximately 20 kHz.  $I_{ROSC}$ , at  $V_{CC} = 14$  V, will be 66.7  $\mu$ A.  $I_{ROSC}$  should not change over a more than 2:1 ratio and therefore  $C_{OSC}$  should be changed to adjust the oscillator frequency.

## Voltage Duty Cycle Conversion

The IC translates an input voltage at the CTL lead into a duty cycle at the OUTPUT lead. The transfer function incorporates ON Semiconductor's patented Voltage Compensation method to keep the average voltage and current across the load constant regardless of fluctuations in the supply voltage. The duty cycle is varied based upon the input voltage and supply voltage by the following equation:

$$\text{Duty Cycle} = 100\% \times \frac{2.8 \times V_{CTL}}{V_{CC}}$$

An internal DC voltage equal to:

$$V_{DC} = (1.683 \times V_{CTL}) + V_{VALLEY}$$

is compared to the oscillator voltage to produce the compensated duty cycle. The transfer is set up so that when  $V_{CC} = 14$  V the duty cycle will equal  $V_{CTL}$  divided by  $V_{REG}$ . For example at  $V_{CC} = 14$  V,  $V_{REG} = 5.0$  V and  $V_{CTL} = 2.5$  V, the duty cycle would be 50% at the output. This would place

a 7.0 V average voltage across the load. If  $V_{CC}$  then drops to 10 V, the IC would change the duty cycle to 70% and hence keep the average load voltage at 7.0 V.

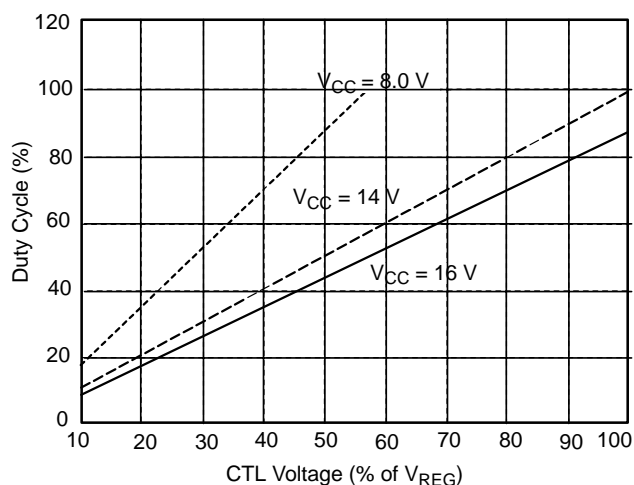


Figure 7. Voltage Compensation

## 5.0 V Linear Regulator

There is a 5.0 V, 5.0 mA linear regulator available at the  $V_{REG}$  lead for external use. This voltage acts as a reference for many internal and external functions. It has a drop out of approximately 1.5 V at room temperature.

## Current Sense and Timer

The IC differentially monitors the load current on a cycle by cycle basis at the  $I_{SENSE+}$  and  $I_{SENSE-}$  leads. The differential voltage across these two leads is amplified internally and compared to the voltage at the  $I_{ADJ}$  lead. The gain,  $A_V$  is set internally and externally by the following equation:

$$A_V = \frac{V_{I(ADJ)}}{I_{SENSE+} - I_{SENSE-}} = \frac{37000}{1000 + R_{CS}}$$

The current limit ( $I_{LIM}$ ) is set by the external current sense resistor ( $R_{SENSE}$ ) placed across the  $I_{SENSE+}$  and  $I_{SENSE-}$  terminals and the voltage at the  $I_{ADJ}$  lead.

$$I_{LIM} = \frac{1000 + R_{CS}}{37000} \times \frac{V_{I(ADJ)}}{R_{SENSE}}$$

The  $R_{CS}$  resistors and  $C_{CS}$  components form a differential low pass filter which filters out high frequency noise generated by the switching of the external MOSFET and the associated lead noise.  $R_{CS}$  also forms an error term in the gain of the  $I_{LIM}$  equation because the  $I_{SENSE+}$  and  $I_{SENSE-}$  leads are low impedance inputs thereby creating a good current sensing amplifier. Both leads source 50  $\mu$ A while the chip is in run mode.  $I_{ADJ}$  should be biased between 1.0 V and 4.0 V. When the current through the external MOSFET exceeds  $I_{LIM}$ , an internal latch is set and the output pulls the gate of the MOSFET low for the remainder of the oscillator cycle (fault mode). At the start of the next cycle, the latch is

reset and the IC reverts back to run mode until another fault occurs. If a number of faults occur in a given period of time, the IC “times out” and disables the MOSFET for a long period of time to let it cool off. This is accomplished by charging the  $C_{FLT}$  capacitor each time an over current condition occurs. If a cycle goes by with no overcurrent fault occurring, an even smaller amount of charge will be removed from  $C_{FLT}$ . If enough faults occur together, eventually  $C_{FLT}$  will charge up to 2.4 V and the fault latch will be set. The fault latch will not be reset until  $C_{FLT}$  discharges to 0.6 V. This action will continue indefinitely if the fault persists.

The off time and on time are set by the following:

$$\text{Off Time} = C_{FLT} \times \frac{2.4V - 0.6V}{4.5 \mu A}$$

$$\text{On Time} = C_{FLT} \times \frac{2.4V - 0.6V}{I_{AVG}}$$

where:

$$I_{AVG} = (295.5 \mu A \times DC) - [4.5 \mu A \times (1 - DC)]$$

$$I_{AVG} = (300 \mu A \times DC) - 4.5 \mu A$$

$$DC = \text{PWM Duty Cycle}$$

### Boost Switch Mode Power Supply

The CS4124 has an integrated boost mode power supply which charges the gate of the external high-side MOSFET to greater than 5.0 V above  $V_{CC}$ . Three leads are used for voltage boost. They are Boost, PMP and SNI. The PMP lead is the collector of a darlington tied NPN power transistor. This device charges the inductor during its on time. The boost lead is the input to chip from the external reservoir capacitor. The SNI lead is the emitter of the power NPN and is connected externally to the  $R_{SNI}$  resistor.

The power supply is controlled by the oscillator. At the start of a cycle an R-S flip flop is set the internal power NPN transistor is turned on and energy begins to build up in the

inductor. The  $R_{SNI}$  resistor sets the peak current of the inductor by tripping a comparator when the voltage across the resistor is 450 mV. The flip flop is reset and the inductor delivers its stored energy to the load. The ripple voltage ( $V_{RIPPLE}$ ) at the Boost lead is controlled by  $C_{BOOST}$ . A snubber circuit, made up of a series resistor and capacitor, is required to dampen the ringing of the inductor. A value of 4.0  $\Omega$  is recommended for  $R_{SNI}$ .

A zener diode is needed between the boost output voltage and the battery. This will clamp the boost lead to a specified value above the battery to prevent damage to the IC. A 9.0 volt zener diode is recommended.

### Sleep State

This device will enter into a low current mode ( $< 275 \mu A$ ) when CTL lead is brought to less than 0.5 V. All functions are disabled in this mode, except for the regulator.

### Inhibit

When the inhibit is greater than 2.5 V the internal latch is set and the external MOSFET will be turned off for the remainder of the oscillator cycle. The latch is then reset at the start of the next cycle.

### Overvoltage Shutdown

The IC will disable the output during an overvoltage event. This is a real time fault event and does not set the internal latch and therefore is independent of the oscillator timing (i.e. asynchronous). There is 325 mV (typical) of hysteresis on the overvoltage function. There is no undervoltage lockout. The device will shutdown gracefully once it runs out of headroom.

### Reverse Battery

The CS4124 will not survive a reverse battery condition. A series diode is required between the battery and the  $V_{CC}$  lead for reverse battery.

### Load Dump

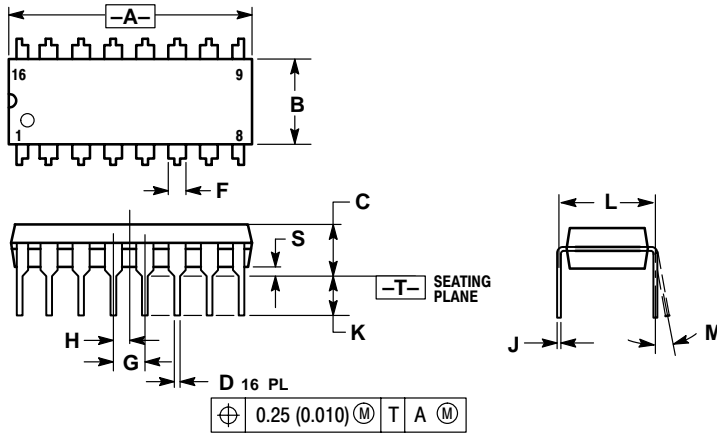
A 10  $\Omega$  resistor, (RS) is placed in series with  $V_{CC}$  to limit the current into the IC during 40 V peak transient conditions.



# CS4124

## PACKAGE DIMENSIONS

DIP-16  
N SUFFIX  
CASE 648-08  
ISSUE R



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

### PACKAGE THERMAL DATA

Parameter		DIP-16	Unit
R <sub>θJC</sub>	Typical	42	°C/W
R <sub>θJA</sub>	Typical	80	°C/W

**Notes**

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